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Alexander E. Mericas

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SYNNESTVEDT & LECHNER, LLP
2600 ARAMARK TOWER
1101 MARKET STREET
PHILADELPHIA, PA 191072950

EXAMINER

WEST, JEFFREY R

ART UNIT

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Please find below and/or attached an Office communication concerning this application or proceeding.



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EXAMINER

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Commissioner for Patents

DETAILED ACTION

Response to Reply Brief

1. The reply brief filed May 22, 2006, has been entered and considered. The application has been forwarded to the Board of Patent Appeals and Interferences for decision on the appeal.

2. The following arguments are also noted:

Appellant argues:

In construing the second prong of the two-part Deminski test cited by the Applicant in the Appeal Brief on page 7, the Examiner incorrectly looks to the claims to determine the particular problem with which the inventor was involved. The Deminski test requires no such evaluation; in this particular case, reference to the specification reveals the problem with which the inventor was involved, as described above, and Dharap is concerned with the display of data on the small screen of a cellular telephone, which has no reasonable pertinence to solving the problem of an inability to use interrupts in certain situations involving hardware testing of a processor.

The Examiner first asserts that it has been held that "the examiner must determine what is 'analogous prior art' for the purpose of analyzing the obviousness of the subject matter at issue. 'In order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned.' This criterion does not indicate that analogy must be considered outside of the claims.

The Examiner also asserts that MPEP § 2141.01(a) describes relevant case law for determining analogy and, specifically with respect to analogy in the electrical arts, describes determining analogy by considering the invention as claimed, specifically:

See, for example, Wang Laboratories, Inc. v. Toshiba Corp., 993 F.2d 858, 26 USPQ2d 1767 (Fed. Cir. 1993) (Patent claims were directed to single in-line memory modules (SIMMs) for installation on a printed circuit motherboard for use in personal computers. Reference to a SIMM for an industrial controller was not necessarily in the same field of endeavor as the claimed subject matter merely because it related to memories. Reference was found to be in a different field of endeavor because it involved memory circuits in which modules of varying sizes may be added or replaced, whereas the claimed invention involved compact modular memories. Furthermore, since memory modules of the claims at issue were intended for personal computers and used dynamic random-access-memories, whereas reference SIMM was developed for use in large industrial machine controllers and only taught the use of static random-access-memories or read-only-memories, the finding that the reference was nonanalogous was supported by substantial evidence.); Medtronic, Inc. v. Cardiac Pacemakers, 721 F.2d 1563, 220 USPQ 97 (Fed. Cir. 1983) (Patent claims were drawn to a cardiac pacemaker which comprised, among other components, a runaway inhibitor means for preventing a pacemaker malfunction from causing pulses to be applied at too high a frequency rate. Two references disclosed circuits used in high power, high frequency devices which inhibited the runaway of pulses from a pulse source. The court held that one of ordinary skill in the pacemaker designer art faced with a rate-limiting problem would look to the solutions of others faced with rate limiting problems, and therefore the references were in an analogous art.).

The Examiner also asserts that the primary reference of Gover is already concerned with interrupt problems, specifically:

With reference now to FIG. 3, there is illustrated a representation of MMCR0 which controls the operation of counters PMC1 and PMC2. As illustrated, MMCR0 is partitioned into a number of bit fields whose settings select events to be counted, enable performance monitor interrupts, and specify the conditions under which counting is enabled. MMCR1, which controls the operation of PMC3 and PMC4, is arranged similarly.

As depicted, bits 0-4 and 18 of MMCR0 determine the scenarios under which PMC1 and PMC2 are enabled to count. By setting bits with appropriate software, a user may enable either or both PMC1 and PMC2, or enable PMC1 initially and enable PMC2 only after PMC1 becomes negative. Bits 5, 16, and 17 are utilized

to control interrupts triggered by PMC1 and PMC2. If an interrupt for a PMC is enabled, an interrupt is generated when the counter becomes negative (i.e., the most significant bit is a 1). Finally, bits 19-25 and bits 26-31 are utilized to select the events monitored by PMC1 and PMC2, respectively. Although PMC1 can monitor 43 different events, and PMC2 can monitor 32 different events, each counter can monitor only one event at a time. According to the method and system of the present invention, the events monitored by PMC1 and PMC2 include not only events generated by units 40-50 of FIG. 2, but also overflows from other PMCs among counters 38. (column 3, lines 18-44)

To monitor access times to memory, the user first sets the appropriate bit fields within MMCR0 utilizing suitable software executed by processor 30. Setting bits 26-31 within MMCR0 instructs performance monitor 32 to monitor accesses to L1 cache 48 and system memory, which is accessed via bus interface unit 50. In addition, by setting other bits within MMCR0, the user selects a threshold number of clock cycles and instructs PMC2 to count the occurrences of accesses which require longer than the threshold number of cycles to complete. By setting bits 19-25 of MMCR0 to select the overflow signal from PMC2 as the event counted by PMC1, the user links PMC1 and PMC2 to form a 32-bit counter. Finally, the user sets bit 17 of MMCR0 to disable the interrupt generated when PMC2 becomes negative. Depending upon the application, the user may choose either to disable or enable the interrupt generated when PMC1 becomes negative by setting bit 16 of MMCR0.

Upon execution of the software under analysis, performance monitor 32 receives signals from L1 cache 48 and bus interface unit 50 via internal bus 52 which indicate accesses to memory. Event detection and counter control logic 34 determines from these signals which accesses require more than the threshold number of cycles to complete. Then, utilizing the values of the bit fields within MMCR0, event detection and counter control logic 34 selects which events are counted among the plurality of inputs to multiplexers 80 and 82 by transmitting control signals 96 and 98. Thus, as determined by the bit values within MMCR0, PMC2 increments in response to memory accesses that require more than the threshold number of cycles to complete and PMC1 counts overflows from PMC2. When the performance analysis terminates at the completion of the software routine or at a user-defined interrupt, PMC1 and PMC2 contain the 32-bit value of the number of memory accesses which required greater than the threshold number of cycles to complete. Utilizing appropriate software commands, a user may then read the count value stored in PMC1 and PMC2. (column 4, lines 17-54)

The Examiner also asserts that, with respect to analogy, the instant specification was considered and, as clearly stated in the Examiner's Answer, described the particular problem presented on page 8, lines 9-16, which states:

Figure 3 is a flowchart illustrating an example of steps performed to allocate PMC's in accordance with a first embodiment of the invention in which the PMC's are divided evenly among the events being monitored. When the number of PMC's and number of events being monitored cannot be divided evenly, one or more of the PMC's will have less than others. Referring to Figure 3, at step 302, the number of events being monitored is determined. At step 304, the number of PMC'S available for monitoring is determined, and at step 306, the number of PMC's available is divided by the number of events to determine the grouping of the PMC's (step 308). (page 8, lines 9-16)

Therefore, the particular problem in which the Appellant is concerned, with respect to the claimed limitations, is not an "interrupt problem" but is instead the problem of performing division and/or item distribution.

The Examiner therefore maintains that since the Deminski test does not indicate that the claims are not to be considered in determining analogy, MPEP § 2141.01(a) describes the determination of analogy with respect to the invention as claimed, the invention of Gover is already concerned with the problem of interrupts, and the specification describes solving a problem of performing division/distribution, which is the same problem solved by Dharap, the invention of Dharap clearly passes the two-part Deminski test.

Appellant argues:

The Examiner implies that Gover, in teaching that a user may configure a performance monitor to monitor up to four events within a data processing

system when the number of occurrences of selected events is anticipated to be less than 2^{16} , also suggests that the provision of a structure that enables the MMCR to calculate the optimal division of the PMCs among the events being monitored. This is simply unsubstantiated by a reasonable reading of Gover. Gover merely teaches that an MMCR can allow control over which PMCs are used to monitor events, and this control enables the ability of certain of the PMCs to be used for overflow of other PMCs. This cannot properly be construed as teaching or suggesting the claimed division calculation of the present invention used to optimize the use of the PMCs.

The Examiner maintains that Gover discloses that when the number of occurrences of selected events is anticipated to be less than 2^{16} , a method is performed for evenly assigning each of the four counting elements (i.e. PMC's) to four separate events to be counted. Gover also discloses that when the number of anticipated event occurrences would cause a single PMC to overflow, a method is performed for evenly assigning each of the four counting elements to the same event to be counted, specifically:

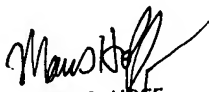
When the maximum number of occurrences of selected events is anticipated to be less than 2^{16} , a user may configure the performance monitor to monitor up to four events within the data processing system. However, if the number of anticipated event occurrences would cause a single PMC to overflow, a user may configure the performance monitor to count up to 2^{64} occurrences without overflow. (column 4, lines 57-64)

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. West whose telephone number is (571)272-2226. The examiner can normally be reached on Monday through Friday, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571)272-2216. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jrw
July 21, 2006


MARC S. HOFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800